WHAT IS CLAIMED IS:

1.   A method comprising:

outputting a first signal having a first frequency that is lower than a desired frequency;

outputting a second signal having a second frequency that is higher than the desired frequency; and

alternating between outputting the first signal and the second signal over a pre-determined time to generate an output signal that is substantially at the desired frequency.

2.   The method of claim 1 wherein alternating between outputting the first signal and the second signal comprises:

generating a first half-cycle of the first signal; and

generating a second half-cycle of the second signal in time series with the first half-cycle of the first signal.

3.   The method of claim 1 wherein alternating between outputting the first signal and the second signal comprises:

generating a half-cycle of the first signal;

stopping generation of the half-cycle of the first signal; and

generating a half-cycle of the second signal.

4.   The method of claim 1 wherein alternating between outputting the first signal and the second signal comprises generating half-cycles of the first signal and the second signal, during the pre-determined time, in a pre-determined ratio to one another.

5.   The method of claim 1 wherein alternating between outputting the first signal and the second signal comprises:

calculating a target value based on the desired frequency and a reference signal;

comparing a count value that is accumulated in a counter in accordance with the reference signal to the target value; and

generating the first signal as long as the count value is less than the target value.

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6.   The method of claim 5 wherein calculating the target value comprises calculating the target value based on a maximum count value expressible by the counter.

7.   The method of claim 5 wherein generating the first signal comprises:
determining that the count value is greater than or equal to the target value; and
switching from outputting the first signal to outputting the second signal.

8.   The method of claim 7 wherein comparing the count value comprises increasing the count value by a pre-determined factor, based on the reference signal.

9.   The method of claim 8 wherein determining that the count value is greater than or equal to the target value comprises:
determining that the count value is greater than the target value;
calculating a remainder of the count value divided by the target value; and
re-setting the counter to an initial count value corresponding to the remainder.

10.   The method of claim 8 wherein determining that the count value is greater than or equal to the target value comprises:
determining that the count value is equal to the target value; and
determining whether a generation time during which the first signal and second signal have been produced is greater than or equal to the pre-determined time.

11.   The method of claim 10 wherein determining whether the generation time is greater than or equal to the pre-determined time comprises:
determining that the generation time is equal to the pre-determined time; and
re-setting the count value to an initial count value of zero.

12.   A system comprising:
a reference clock operable to output a reference signal;
a counter operable to increase a count value with reference to the reference signal;

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a comparison circuit operable to compare the count value with a target value and output a corresponding comparison signal; and

an output circuit operable to alternately output a first signal having a first frequency and a second signal having a second frequency, based on the comparison signal,

5   wherein the first signal and the second signal, being alternately output over a pre-determined time period, result in an output signal substantially having a desired frequency.

13.   The system of claim 12 wherein the first frequency is lower than the desired frequency and the second frequency is higher than the desired frequency.

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14.   The system of claim 12 wherein the output circuit outputs the first signal and the second signal in time series with one another and in a pre-determined ratio to one another.

15   15.   The system of claim 12 wherein the target value is determined based on a maximum count value expressible by the counter.   .

16.   The system of claim 12 wherein the output circuit initially outputs the first signal when the comparison signal indicates that the count value is less than the target value.

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17.   The system of claim 12 wherein the counter is operable to increase the count value by a pre-determined factor and in accordance with the reference signal, as long as the count value is less than the target value.

25   18.   The system of claim 17 wherein the intermediate output circuit switches from outputting the first signal to outputting the second signal when the comparison signal initially indicates that the count value is greater than or equal to the target value.

19.   The system of claim 18 further comprising a counter re-set circuit operable to
30   receive information that the count value is greater than or equal to the target value, and re-set

the counter to an initial count value corresponding to a remainder of the count value divided by the target value.

20. The system of claim 12 comprising a timer operable to determine whether the pre-determined time period has elapsed during outputting of the first signal and the second signal by the output circuit.

21. A system comprising:

a measuring subsystem operable to measure a variable;

a mapping subsystem operable to map the variable to a corresponding frequency;

a frequency generator operable to generate a first frequency that is lower than the desired frequency and a second frequency that is higher than the desired frequency, and further operable to alternately output the first frequency and the second frequency to obtain an output signal having an output frequency substantially equal to the corresponding frequency; and

a transmitter operable to transmit the output signal.

22. The system of claim 21 wherein the frequency generator comprises:

a reference clock operable to output a reference signal;

a counter operable to repetitively increase a count value contained therein by a pre-determined incremental amount, based on the reference signal; and

an output circuit operable to output the first frequency while the count value is less than a pre-determined value, and to switch to outputting the second frequency once the count value is greater than or equal to the pre-determined value.

23. The system of claim 22 wherein the output circuit is further operable to:

determine that the count value is greater than or equal to the target value;

perform a division of the count value by the target value, and determine a remainder of the division; and

re-set the counter to an initial count value equal to the remainder.

24.   A method of generating an output signal having a desired frequency, the method comprising:

calculating a target value based on the desired frequency and a reference signal;

comparing a first count value to the target value, where the first count value is

5   progressively accumulated in a counter in accordance with the reference signal;

outputting a first output value as long as the first count value is less than the target value;

determining that the first count value has become a current count value that is greater than or equal to the target value;

10   calculating a remainder of a division of the current count value by the target value;

re-setting the counter at an initial count value that is based on the remainder; and

outputting a second output value, whereby the output signal is obtained.

25.   The method of claim 24 further comprising:

15   counting a second count value from the initial count value, while outputting the second output value;

determining that the second count value is greater than or equal to the target value; and

outputting the first output value.

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26.   The method of claim 24 wherein comparing the first count value to the target value comprises progressively accumulating the first count value according to a pre-determined increment.

25   27.   The method of claim 24 wherein re-setting the counter comprises re-setting the initial count value to be equal to the remainder.